

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	35743	reconfigur\$4 and table	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 08:34
L2	3673	reconfigur\$4 same table	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 08:35
L3	224	reconfigur\$4 same table.ab.	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 08:35
L4	3	reconfigur\$4 same load\$4 near3 table.ab.	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 08:36
L5	19	reconfigur\$4 same load\$4 near3 table same address\$4	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 08:37
L6	0	4 and 5	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 08:37
L7	21	reconfigur\$4 same table near5 address\$4 and (713/?ccls. 711/?ccls. 326/3?ccls.)	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:16
L8	6	reconfigur\$4 same table near5 address\$4 and (preserv\$4 sav\$3) and (713/?ccls. 711/?ccls. 326/3?ccls.)	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:22
L9	660	(sav\$4 preserv\$4) near2 configuration same load\$4	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:30

L10	326	(sav\$4 preserv\$4) near2 configuration same load\$4 and g06f\$.ipc.	US- PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:30
L11	18	(sav\$4 preserv\$4) near2 configuration same load\$4 same logic and g06f\$. ipc.	US- PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:31
L12	20	table with (preserv \$4 sav\$4) same (\$2configur\$5 near2 logic) and g06f\$.ipc.	US- PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:32
L13	95	(preserv\$4 sav\$4) near5 (\$2configur \$5 near2 logic) and g06f\$.ipc.	US- PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:33
L14	2	(preserv\$4 sav\$4) near5 (\$2configur \$5 near2 logic) near4 load\$4 and g06f\$.ipc.	US- PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:34
L15	1	"6282627".pn.	US- PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:47
L16	18	(sav\$4 preserv\$4) near2 configuration same load\$4 and FPGA.ab. and g06f \$.ipc.	US- PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:50
L17	17	(sav\$4 preserv\$4) near2 configuration same load\$4 and FPGA.ab. and (external\$4 off \$1chip) and g06f\$. ipc.	US- PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:55

L18	0	(sav\$4 preserv\$4) near2 configuration same load\$4 and FPGA.ab. and (external\$4 off \$1chip) near2 address\$3 and g06f\$.ipc.	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/14 09:56
S1	172615	(phillips wong)".in. and" configuration adj plane\$1.dm.	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/10 15:27
S2	5	(phillips wong).in. and configuration adj plane\$1.dm.	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/10 15:27
S3	6	"728551".ap.	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/10 17:52
S4	1	"728551".ap. and sav\$4 same load \$4	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/10 17:52
S5	1	"728551".ap. and on\$1chip adj configuration adj plane\$1	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/10 17:54
S6	1	"728551".ap. and configuration adj plane\$1	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/10 17:54
S7	1	"728551".ap. and plane with off \$1chip	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/10 18:08
S8	3	"728551".ap. and table	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2008/10/10 18:09

10/ 14/ 08 9:56:41 AM

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 \10728551A2 - FPGA with bootable off-chip configuration.wsp